TC8505AP/F

(Cathode Ray Tube Display Controller)

INTRODUCTION

The TC8505AP/F CRT Controller is a single-chip CMOS LSI developed for the purpose of interfacing with a raster scan type CRT display, and is used on MPU, CRT, terminal units, etc.

The TC8505AP/F is a higher speed version of TC8505P/F with same function. The CLOCK frequency is 6MHz maximum, therefore the higher resolution CRT display can be constructed easily by the TC8505AP/F.

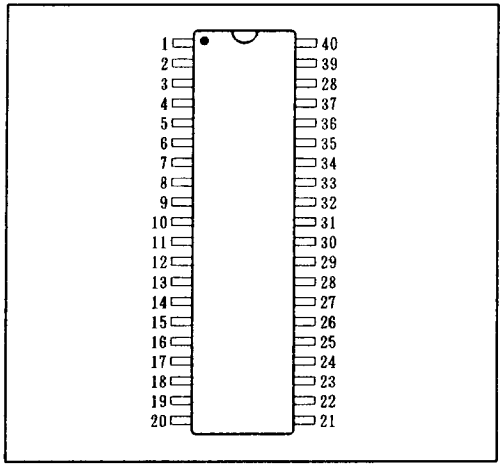
The key-board function, read, write, cursor control, and edit are all controlled by a processor. The CRTC generates display timing and refresh memory address output. The any type of the $^{O\cdot T}$ display can be realized by optimising the CRTC with well balanced haedware/software.

FEATURES

- o Silicon-gate CMOS Construction
- o Single +5V Power Supply
- o 40 pin DIP and 44 pin miniFP
- o 6 MHz High-Speed Display Operation
- o TTL compatible Inputs and Outputs
- o Full Static Function
- o Programmable Number of Display Characters, Number of Rasters per Line, Display Position, Horizontal and Vertical Timing, etc.
- o Programmable Cursor Position, Format and Blinking
- o No Line Buffer is Required for Refreshing the Screen.
- o Output of 14-bit Refresh Memory Address (Max. 16K words accessible)
- o Three Selectable Scan Modes of Interlace, Non-interlaced Sync, and Interlace & Video.
- o Programmable Display Start Address (applicable to paging, scrolling, etc.)
- o Built-in Light Pen Detecting Function
- o Functionally Compatible with MOTROLA MC6845 and HITACHI HD46505S.

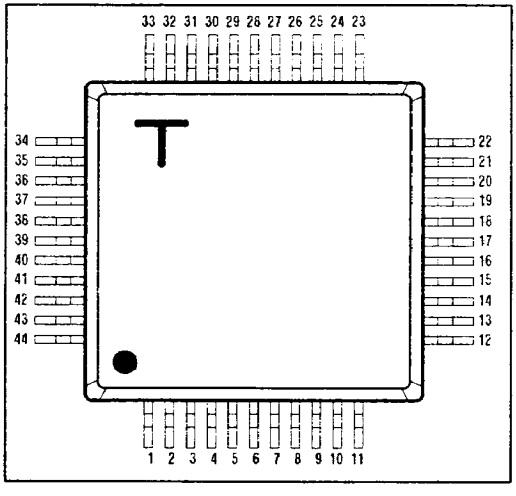
PIN CONFIGURATION

TC8505AP



PIN NO.	IO	PIN NAME	PIN NO.	IO	PIN NAME
1	G	GND	21	I	CLOCK
2	I	/RESET	22	I	R/W
3	I	LPSTB	23	I	E
4	O	RMA0	24	I	RS
5	O	RMA1	25	I	/CS
6	O	RMA2	26	IO	DB7
7	O	RMA3	27	IO	DB6
8	O	RMA4	28	IO	DB5
9	O	RMA5	29	IO	DB4
10	O	RMA6	30	IO	DB3
11	O	RMA7	31	IO	DB2
12	O	RMA8	32	IO	DB1
13	O	RMA9	33	IO	DB0
14	O	RMA10	34	O	SLA4
15	O	RMA11	35	O	SLA3
16	O	RMA12	36	O	SLA2
17	O	RMA13	37	O	SLA1
18	O	DISPE	38	O	SLA0
19	O	CURDISP	39	O	HSYN
20	V	(VCC)	40	O	VSYN

TC8505AF

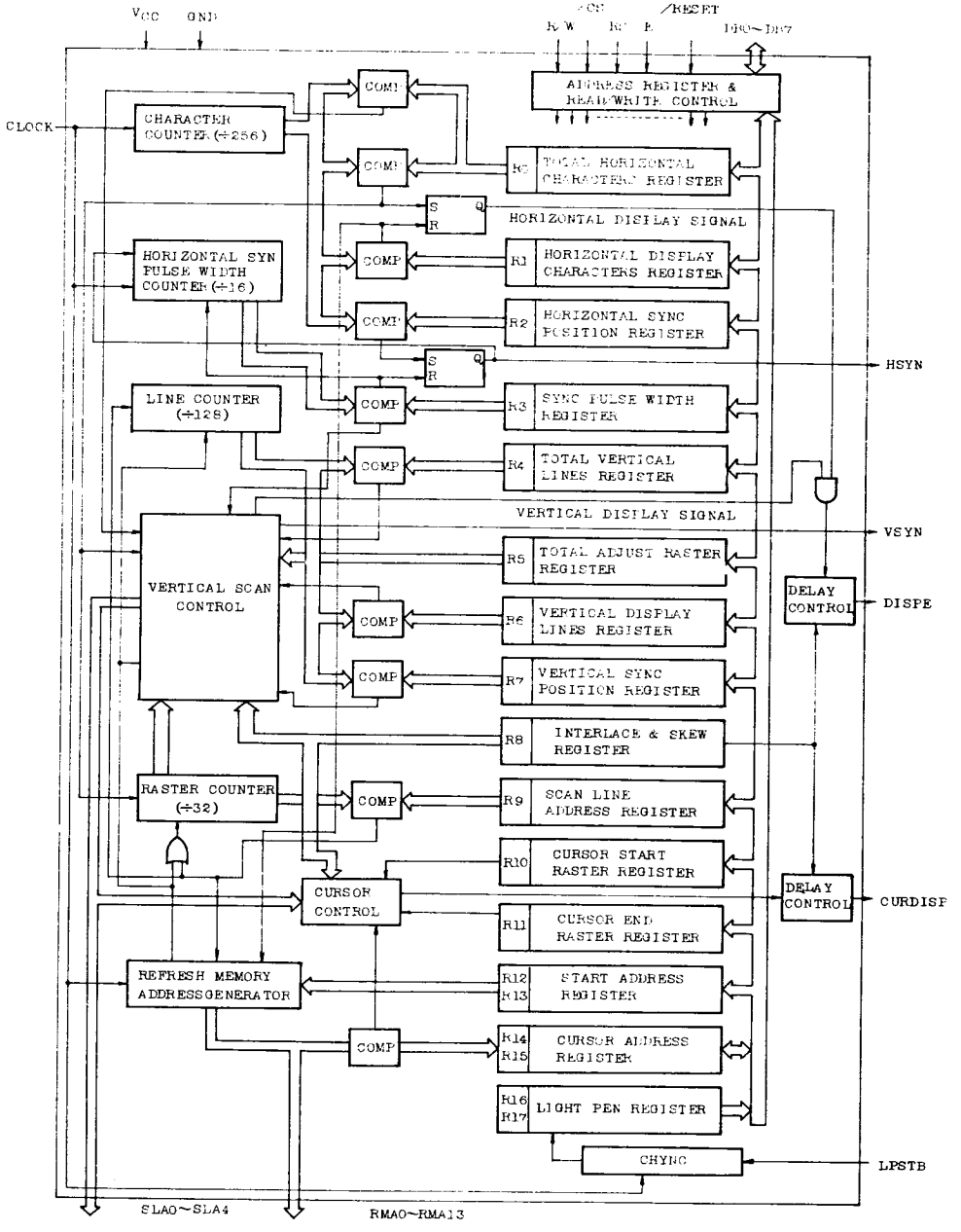


PIN NO.	IO	PIN NAME	PIN NO.	IO	PIN NAME
1	O	RMA1	23		NC
2	O	RMA2	24	IO	DB7
3	O	RMA3	25	IO	DB6
4	O	RMA4	26	IO	DB5
5	O	RMA5	27	IO	DB4
6	O	RMA6	28	IO	DB3
7	O	RMA7	29	IO	DB2
8	O	RMA8	30	IO	DB1
9		NC	31	IO	DB0
10	O	RMA9	32	O	SLA4
11	O	RMA10	33	O	SLA3
12	O	RMA11	34	O	SLA2
13	O	RMA12	35	O	SLA1
14	O	RMA13	36	O	SLA0
15	O	DISPE	37	O	HSYN
16	O	CURDISP	38	O	VSYN
17	V	(VCC)	39	V	(VCC)
18	I	CLOCK	40	G	GND
19	I	R/W	41	I	/RESET
20	I	E	42	I	LPSTB
21	I	RS	43	O	RMA0
22	I	/CS	44		NC

FUNCTIONAL DESCRIPTION OF TERMINALS

- DB0 - DB7 (Data Bus) Input/Output
  The bidirectional data bus for exchanging data with CPU.
- R/W (Read/Write) Input
  When "High", CRTC data is transferred to CPU, while data is transferred from CPU to CRTC when "Low".
- E (Enable) Input
  CRTC enables the data bus and signal exchange with CPU at the edge from "High" to "Low". Clock signal from CPU is generally used.
- RS (Register Select) Input
  The address register is selected when "Low", and the data register is selected when "High".
- /CS (Chip Select) Input
  When "Low", CRTC is selected to enable read/write by CPU.
- CLOCK (Clock) Input
  This terminal is used for synchronizing signals for all operations except for interface with CPU. Generally, an external dot counter is used and which give character rate in a character display CRT.
- /RESET (Reset) schmitt Trigger Input
  CRTC reset signal input. All counters of CRTC are initialized and display operation is stopped but the contents of the control register remain without being affected.
  * CAUTIONS:
    1) When "LPSTB" is at "High", the reset operation is not carried out. (At this time, the test mode results.)
    2) After "/RESET" has been "Low", RMA0 to RMA13 and SLA0 to SLA4 go "Low" at the falling edge of "CLOCK" signal. Therefore, "/RESET" must be kept at "Low" level for at least one cycle of "CLOCK" signal.
    3) Immediately after "/RESET" is released, CRTC resumes the display operation. However, "DISPE" is not output until the first "VSIN"(Vertical Sync) is output.

- LPSTB (Light Pen Strobe) Schmitt Trigger Input
  When this input transits from "Low" to "High", the refresh address are latched in the light pen register. The latch of the refresh address is executed synchronizing with "CLOCK" signal.
- VSYN (Vertical Sync) Output
  Vertical synchronizing signal is given to CRT.
- HSYN (Horizontal Sync) Output
  Horizontal synchronizing signal is given to CRT.
- DISPE (Display Enable) Output
  When at "High" level, it indicators that the CRT is under the display.
- RMA0 - RMA13 (Refresh Memory Address) Output
  Memory address to refresh the CRT screen is provided. The refresh memory with pages of data stored within a 16K block is accessible.
- SLA0 - SLA4 (Scan Line Address) Output
  Scan line address is output to a character generator, etc.
- CURDISP (Cursor Display Signal) Output
  Effective cursor address for displaying the cursor is output to an external display unit.



CRTC Internal Block Diagram

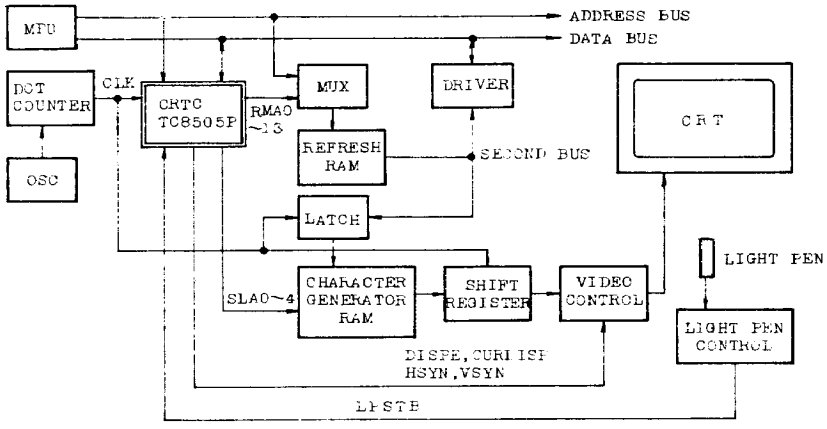


Fig.1 CRT Controller System Configuration Example

DESCRIPTION OF CRTC DISPLAY SYSTEM

The CRT Controller provides required signal to a raster scan type CRT display circuit. On such a display as this, the electron beam starts from the upper left corner, crosses the screen, and returns back. This movement of the electron beam is called a horizontal scan. The electron beam gradually moves down in the vertical direction for every horizontal scan to the bottom of the screen. When the electron beam has reached the bottom of the screen, one frame is displayed by many horizontal scans and one vertical scan.

Two scanning line systems of interlace and non-interlace are used in CRTs. In the non-interlace scan mode (Fig.2), one frame is displayed in one field. In Fig.2, the solid line represents the scan line while the dotted line indicates the retrace line. When number of pictures per second is increased, flicker of the frame is reduced. Normally, the refreshing rate of 50 or 60 frame/sec is used to minimize the beat between CRT and supply frequency.

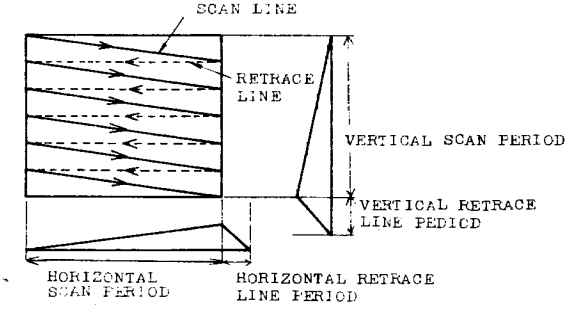


Fig.2 Raster Scan System (Non-Interlace)

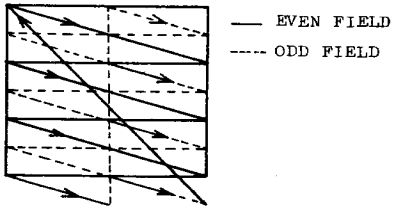


Fig.3 Raster Scan System (Interlace)

The interlace scan mode is used for TV, and monitors which require high density and high resolution. One picture (one frame) is made by two fields (two times of the vertical scan). The first field (the even field) starts from the upper left corner. The second field (the odd field) starts from the upper center. As shown in Fig.3, two fields interlace into single frame.

The frames must be constantly repeated to display characters on the CRT screen. Display data is stored in the refresh memory through the control of the data processing circuit by MPU. This data is usually written in ASCII codes and cannot be displayed directly as a character. Therefore, the character generator ROM is generally used to convert ASCII codes into a dot pattern for every character.
MPU interfaces with CRTC through an 8-bit data bus by performing write or read into 19 registers.

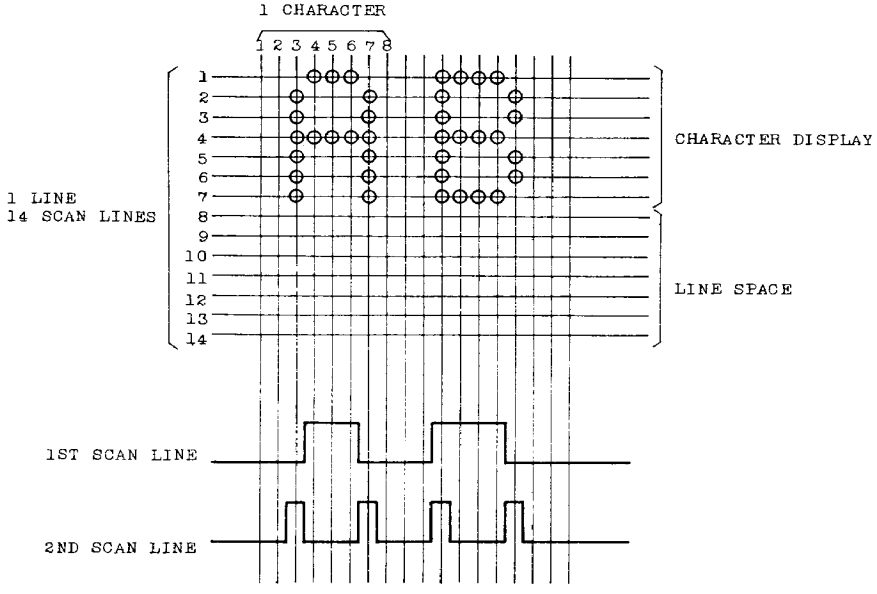


Fig.4 Character Display on Screen and Video Signal

A common method of generating characters is to create a dot matrix by x dots (columns) and y dots (rows). Each character consists of dots in predetermined arrangement. More detailed characters can be constructed by increasing number of x and y dots. The dot matrix of 5x7 or 7x9 is general. These constructions make possible to construct many variations using Chinese, Japanese, or arabic letters instead of the alphabet. Since a space is required between characters as shown in Fig.4, a block of characters becomes larger than a block usually occupied by characters. Timing and level of video signal are also shown in this figure.

Fig.1 shows an example of general CRT controller system configuration. The CRTC provides refresh memory addresses (RMA0-13), scan line addresses (SLA0-4) and video timing signals (HSYN, VSYN, DISPE). In addition, the CRTC has such functions as the cursor register providing CURDISP by comparing with refresh addresses, light pen register by catching refresh addresses by the light pen strobe (LPSTB), etc.

All timings of CRTC are derived from CLOCK input. This clock is character rate at the character display terminal. Display speed or dot clock is supplied to CLOCK input by the external circuit. This external circuit also produces timing to control the shift register, latch, and MUX (multiplexer).

		Address Reg.						Reg.	Register Name	Program	Symbol	Write	Data Bit							
CS	RS	4	3	2	1	0		No.		Unit		or Read	7	6	5	4	3	2	1	0
1	X	X	X	X	X	X		-	Nullification	-	-	Write	X	X	X	X	X	X	X	X
0	0	X	X	X	X	X		AR	Address Register	-	-	Write	X	X	X					
0	1	0	0	0	0	0		R0	Total Horizontal Characters	Character	Nht	Write								
0	1	0	0	0	0	1		R1	Horizontal Display Characters	Character	Nhd	Write								
0	1	0	0	0	1	0		R2	Horizontal Sync Position	Character	Nhsp	Write								
0	1	0	0	0	1	1		R3	Sync Pulse Width (V, H)	Raster, Charac.	Nvw Nhw	Write	Vw3	Vw2	Vw1	Vw0	Hw3	Hw2	Hw1	Hw0
0	1	0	0	1	0	0		R4	Total Vertical Lines	Line	Nvt	Write	X							
0	1	0	0	1	0	1		R5	Total adjust Raster	Raster	Nadj	Write	X	X	X					
0	1	0	0	1	1	0		R6	Vertical Display Lines	Line	Nvd	Write	X							
0	1	0	0	1	1	1		R7	Vertical Sync Position	Line	Nvsp	Write	X							
0	1	0	1	0	0	0		R8	Interlace & Skew			Write	C1	C0	D1	D0	X	X	V	S
0	1	0	1	0	0	1		R9	Scan Line Address	Raster	Nr	Write	X	X	X					
0	1	0	1	0	1	0		R10	Cursor Start Raster	Raster	Ncsta	Write	X	B	P					
0	1	0	1	0	1	1		R11	Cursor End Rasters	Raster	Ncend	Write	X	X	X					
0	1	0	1	1	0	0		R12	Start Address (H)		-	R/W	X	X						
0	1	0	1	1	0	1		R13	Start Address (L)		-	R/W								
0	1	0	1	1	1	0		R14	Cursor Address (H)		-	R/W	X	X						
0	1	0	1	1	1	1		R15	Cursor Address (L)		-	R/W								
0	1	1	0	0	0	0		R16	Light Pen Address (H)		-	Read	X	X						
0	1	1	0	0	0	1		R17	Light Pen Address (L)		-	Read								

* Raster = Horizontal Scan Line

* Caution Write a value of designated value minus 1 (-1) into each of R0, R2, R4 and R7 registers, respectively.

Address Register (AR)

This is a 5-bit address register to give addresses of the control registers. When both RS and /CS are "Low", the address register is selected. When /CS is "Low" and RS is "High", the control register pointed by the address register is selected.

Control Registers (R0-R13)

Shown in Fig.5 is a general display area on a CRT monitor which composed of according to the contents of the timing registers. The registers for horizontal scan (R0-R3) are programmed with character used as the unit. These timings are shown in Fig.6. The difference between (R0) and (R1) means the horizontal blanking period. The beam returns to the left end of the screen within this period. Though this retrace line period is determined by the specification of horizontal scan for respective monitors, it is generally positioned at the center of the blank period of horizontal scan. The registers for vertical scan (R3-R9) are programmed with using raster or line as units. These timings are shown in Fig.7.

Total Horizontal Characters (R0)

This is an 8-bit register defining the horizontal sync frequency by specifying the horizontal scan period with the total number of characters per line. A value of total horizontal number of characters minus 1 (-1) is written into this register. In case of the interlace mode it is necessary to determine characters so that total horizontal number of characters is an even number.

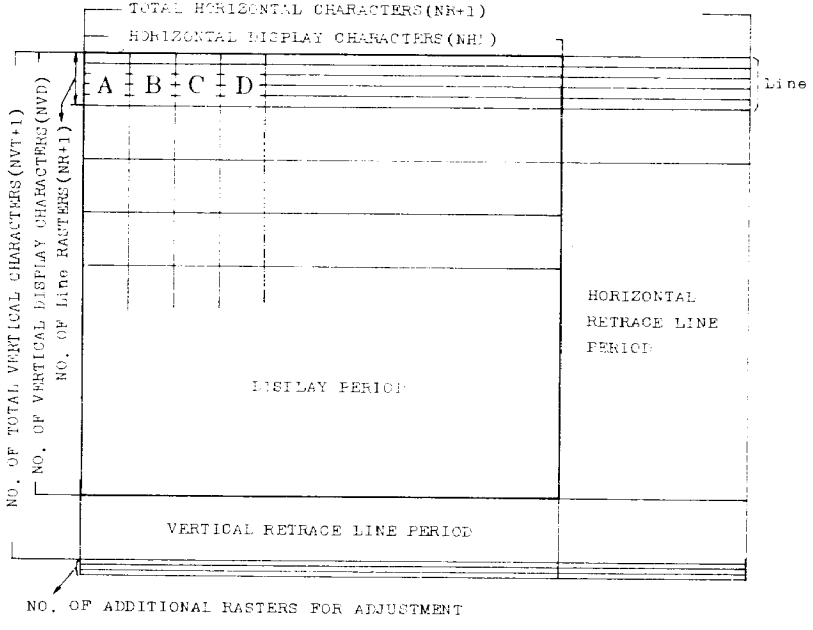


Fig.5 CRT Screen Construction Diagram

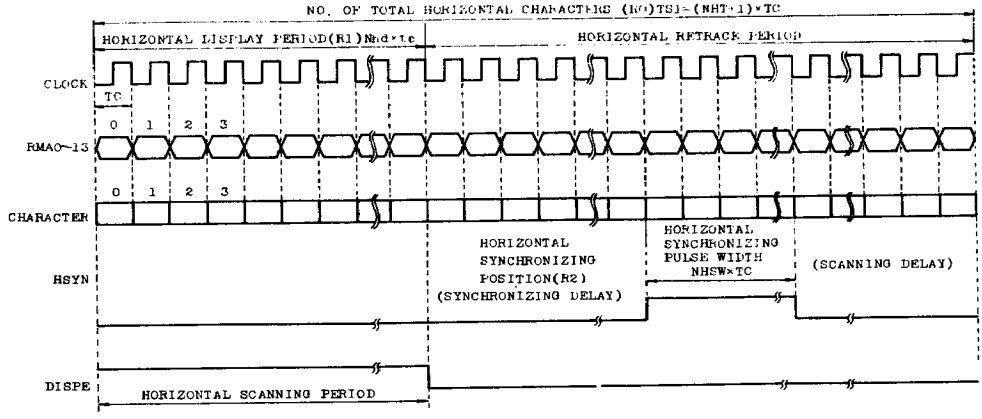


Fig.6 Horizontal Scanning Timing Chart

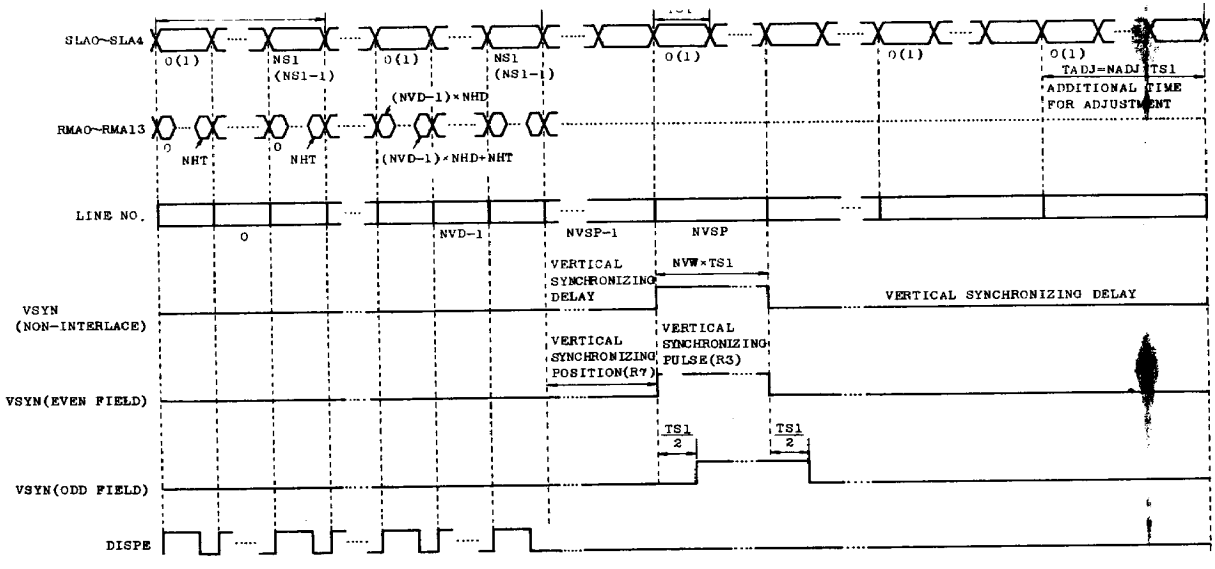


Fig.7 Vertical Scanning Timing Chart

Horizontal Display Characters (R1)

This is a 8-bit register determining number of display characters per line. A value less than number of total horizontal characters should be set.

Horizontal Sync Position (R2)

This is a 8-bit register controlling position of horizontal sync signal (HSYN). The horizontal sync position defines the horizontal sync delay period and horizontal scan delay period. When this set value is increased, the display on the CRT is shifted to the left. When it is decreased, the display is shifted to the right. Total of set values of (R1), (R2) and (R3) should be so programmed smaller than a value of (R0).

Sync Pulse Width (R3)

This is a 8-bit register determining pulse width of the horizontal sync (HSYN) and vertical sync (VSYN). Pulse width of the vertical sync is set up by high order 4 bits. When "0" is set, 16 rasters are resulted. Low order 4 bits set up pulse width of the vertical sync in 1 to 14 characters. When "0" is set, no horizontal sync is generated.

Total Vertical Lines (R4)

This is a 7-bit register providing number of lines required for determining the vertical scanning cycle. A value of total number of vertical lines minus 1 (-1) should be written into this register.

Total Adjust Rasters (R5)

In order to adjust vertical scan frequency to just 50Hz or 60Hz, it is necessary to add mumber of rasters that cannot be specified by the number of total vertical character lines register (R4). This is a 5-bit register for determining this number of raster to be added.

Vertical Display Lines (R6)

This is a 7-bit register specifying number of character lines that are displayed on the screen. A number less than total vertical lines should be programed.

Vertical Sync Position (R7)

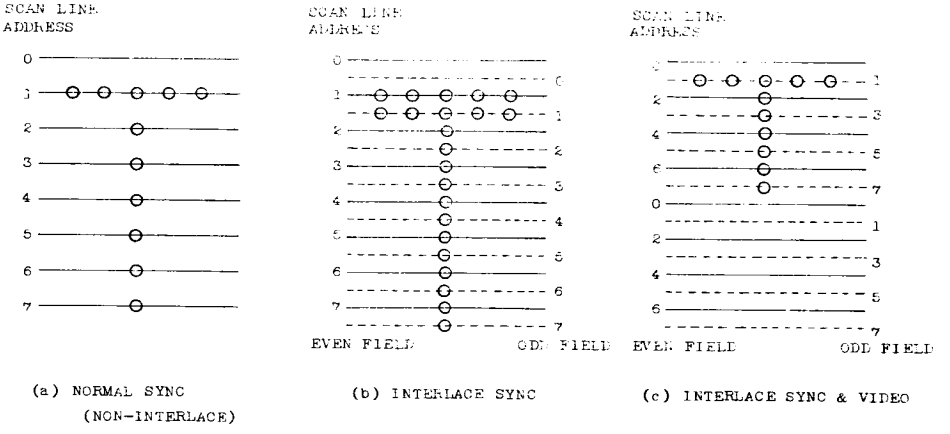
This is a 7-bit register determining the position of vertical sync signal by number of lines. the number to be programed is one less than the number to be set. When a number set in this register is increased, the display position on the screen is shifted upward and when it is decreased, the position is shifted downward. A number equal to or smaller than total number of vertical lines should be set up.

Interlace & Skew (R8)

This is a register for select a scan line mode and specifying delay (skew) of DISPE and CURDISP outputs. Bits 6 and 7 of this register specify DISPE output delay (skew) while Bits 4 and 5 specify CURDISP output delay (skew) in 2 characters starting from 0. If 3 is programed, that signal is not output. A scan mode is selected by Bit 0 and Bit 1 (V, S). Scan modes corresponding to contents of bits are shown in Table 2.

Bit 1 V	Bit 0 S	Scan line mode
X	0	Non interlace mode
0	1	Interlace Sync mode
1	1	Interlace Sync & video mode

Table 2 Interlace Mode Register (R8)



(a) NORMAL SYNC (NON-INTERLACE) (b) INTERLACE SYNC (c) INTERLACE SYNC & VIDEO

Fig.8 Interlace Control

In the normal sync (non-interlace) mode, only one time field is valid as illustrated in Fig.2 and Fig.8. One frame is refreshed by the vertical sync signal frequency.
In two interlace modes, the field is divided into the even field and odd field which appear alternately as shown in Fig.3 and Fig.8.
In the interlace sync mode, the same one is drawn in two fields as illustrated in Fig.8(b) and it is easy to read sentences.
In the interlace sync & video mode, a character is displayed by the alternate scanning lines of the even and odd fields as illustrated in Fig.8(c) and the frequency band given to CRT monitor can be thus doubled.

Scan Line Address (R9)

This is a 5-bit register defining scan line times per character row including line space, and maximum scan line addresses is decided. (Specified Value)-1 should be programmed for the non-interlace mode and (Specified Value)-2 for the interlace sync & video mode. Further, in case of the interlace sync & video mode, the sum of scan lines of the even field and those of the odd field is number of scan lines per line as illustrated in Fig.8.

Cursor Start Raster (R10), Cursor End Raster (R11)

These registers are for controlling the range of scan lines displaying the cursor in the character block and the display state of the cursor as shown in Fig. 9. (R10) specifies the cursor display start raster by low order 4 bits and the cursor display mode by Bit 5 and Bit 6 as shown in Table 3. (R11) is a 5-bit register specifying the last raster of cursor display.

Bit 6 B	Bit 5 P	Cursor display mode
0	0	Does not blink
0	1	The cursor is not displayed
1	0	Blinks in 16 field time
1	1	Blinks in 32 field time

Table 3 Cursor Display Mode Register (R10)

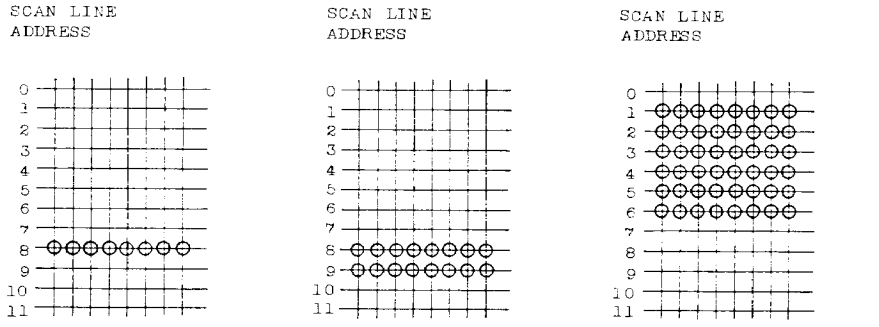


Fig. 9 Cursor Control

Start Address (R12), (R13)

These are total 14 bits registers controlling an address value that is first output of CRTC after the vertical blank period. Low order addresses of RMA0 to RMA7 are set by 8 bits of (R13) and high order addresses of RAM8 to RAM13 by 6 bits of (R12). According to the contents of this start address register, that portion of the refresh RAM, which is displayed on the CRT screen, is determined and thus, the scrolling for each character, line or page can be easily realized.

Cursor Address (R14), (R15)

These are total 14 bits registers determining the refresh RAM address of the cursor display position. These are possible to read from CPU. Low order addresses of RMA0 to RMA7 are set by 8 bits of (R15), and high order addresses of RMA8 to RMA13 by 6 bits of (R14).

Light Pen Address (R16), (R17)

These are total 14 bits registers catching refresh address that is output by the CRTC at the rising edge of pulse to LPSTB input, and is used exclusively for read from CPU. Low order addresses of RMA0 to RMA7 are held by 8 bits of (R17) and high order addresses of RMA8 to RMA13 by 6 bits of (R16). Since the light pen pulse is asynchronous with the refresh address timing, they are synchronized in the CRTC. It is therefore necessary to correct delay time shown in Fig. 10 and delay time of the entire light pen detection circuit, that is, delay of refresh address output, delay involved after light emission by CRT until light detection and pulse generation by the light-pen, etc. by software.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

ITEM	SYMBOL	RATING	UNIT
Supply Voltage	VCC	-0.5 + 7.0	V
Input Voltage	VIN	-0.5 to Vcc + 0.5	V
Operating Temperature	Topr	-40 to + 85	°C
Storage Temperature	Tstg	-65 to + 125	°C

DC CHARACTERISTICS

VCC = 5V ± 10%, Ta = -40 to + 85°C

PARAMETER	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT
Input Low Voltage	VIL		0	0.8	V
Input High Voltage	VIH		2.2	Vcc	V
Output Low Voltage	VOL	IOL = 2.2mA	-	0.4	V
Output High Voltage	VOH	IOH = -1.1mA	Vcc-0.4	-	V
Output Float Leak Current	IFL	VOUT= 0v to Vcc	-10	+10	uA
Input Leak Current	IIL	VIN = 0v to Vcc	-10	+10	uA
Supply Current	Icc		-	10	mA

AC CHARACTERISTICS

1. CRT Control Signal Timing

Vcc = 5V ± 10%, Vss = 0V, Ta = -40 to + 85°C

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT
Clock Cycle Time	tcycc		160	-	nS
"High" Clock Pulse Width	PWCH		70	-	nS
"Low" Clock Pulse Width	PWCL		70	-	nS
Clock Rise/Fall Time	PWCL		-	20	nS
Memory Address Delay Time	tRMAD		-	110	nS
Scanning Line Address Delay Time	tSLAD		-	110	nS
DISPE Delay Time	tDTD		-	110	nS
CURDISP Delay Time	tCDD		-	110	nS
Horizontal Sync Delay Time	tHSD		-	100	nS
Vertical Sync Delay Time	tVSD		-	110	nS
Light Pen Strobe Pulse Width	PWLPH		40	-	nS
Light Pen Strobe Disable Time	tLPD1		-	50	nS
	tLPD2		-	0	nS

2. **BUSS TIMING CHARACTERISTICS**

Vcc=5V ± 10%, Vss=0V, Ta=-40 to + 85°C

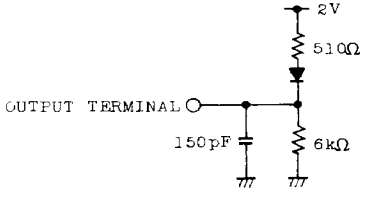
MPU READ TIMING

PARAMETER	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT
Enable Cycle Time	tCYCE		250	-	nS
"High" Enable Width	PWEH		120	-	nS
"Low" Enable Width	PWEL		120	-	nS
Enable Rise/Fall Time	tEr,tEf		-	20	nS
Address Set-up Time	tAS		20	-	nS
Data Delay Time	tDDR		-	100	nS
Data Holding Time	tDH		10	-	nS
Address Holding Time	tAH		10	-	nS
Data Access Time	tACC		-	120	nS

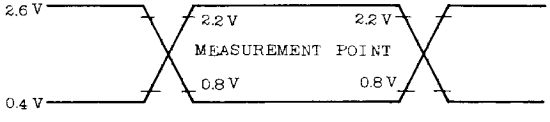
MPU WRITE TIMING

PARAMETER	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT
Enable Cycle Time	tCYCE		250	-	nS
"High" Enable Width	PWEH		120	-	nS
"Low" Enable Width	PWEL		120	-	nS
Enable Rise/Fall Time	tEr,tEf		-	20	nS
Address Set-up Time	tAS		20	-	nS
Data Delay Time	tDDR		60	-	nS
Data Holding Time	tDH		10	-	nS
Address Holding Time	tAH		10	-	nS

Loading Condition in External Terminal



Input Waveform for AC TEST



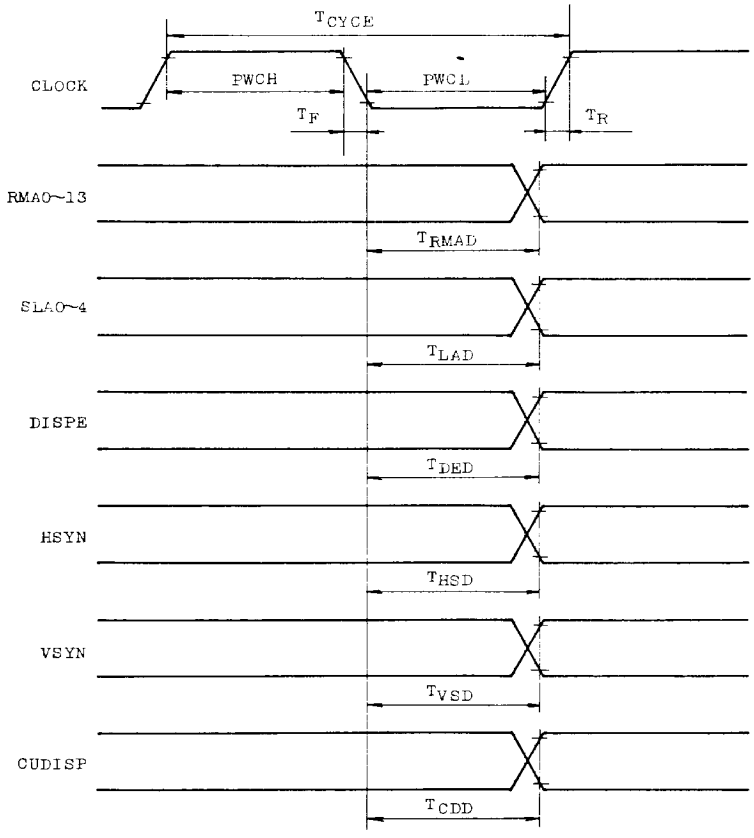


Fig. 10 Output Signal Timing

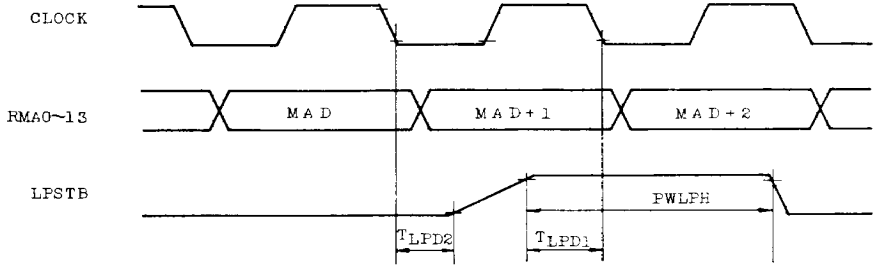
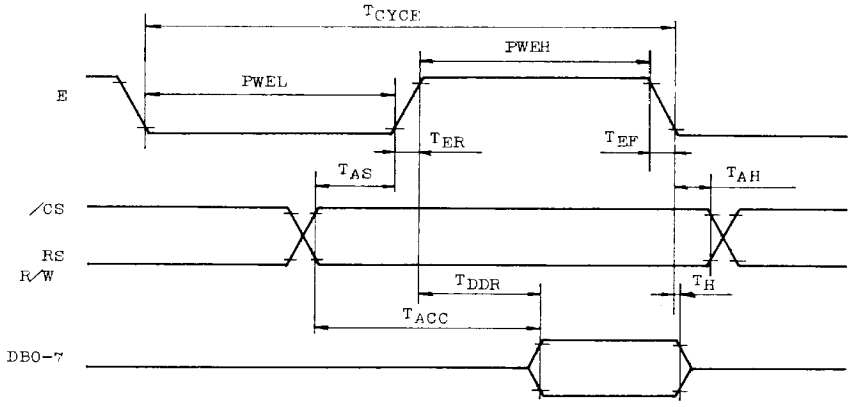


Fig. 11 Light Pen Strobe Timing

Read Timing



Write Timing

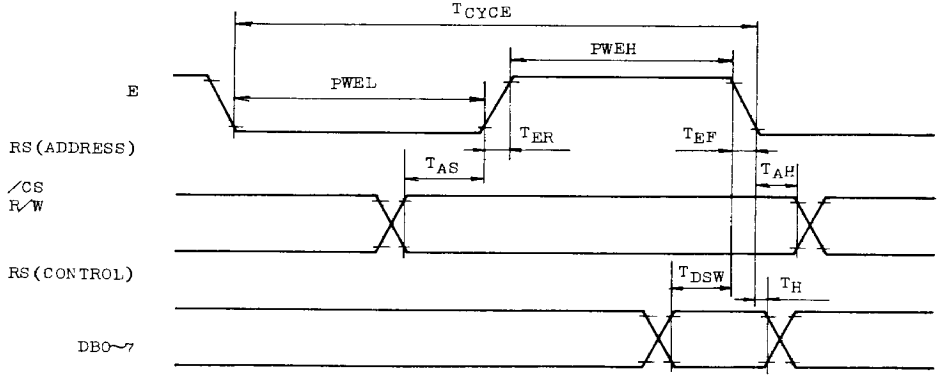
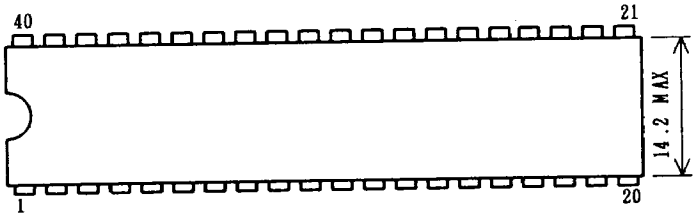


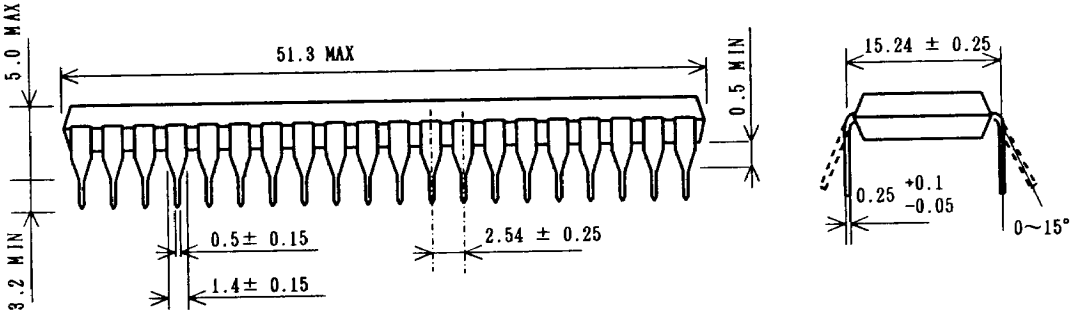
Fig. 12 Bus Timing

PACKAGE OUTLINE

DIP 40 PIN (PLASTIC PACKAGE)

Unit: mm





44 PIN mini FP

Unit: mm